



S/N 09/608,645

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Brian M. Leitner et al.	Examiner:	Aaron N Strange
Serial No.:	09/608,645	Group Art Unit:	2153
Filed:	June 30, 2000	Docket No.:	884.957US1
Title:	MEMORY UTILIZATION IN A NETWORK INTERFACE		
Assignee:	Intel Corporation	Customer No:	21186

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Office Action mailed May 11, 2005, the Applicant requests review of the rejections in the above-identified application. The pending claims in the above identified application stand twice rejected, wherein no amendments were made to the claims in response to the previous Final Office Action mailed June 17, 2004, and no amendments to the claims were made in submitting a Request for Continued Examination (RCE) in the above identified application, the RCE being mailed on February 17, 2005, the unamended claims being again rejected in the currently pending Office Action. Further, no amendments are submitted with this request, which is being filed with a Notice of Appeal, and for the reasons stated below.

§102 Rejection of the Claims

Claims 1-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Muller et al. (U.S. 6,453,360). Claims 19-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dobecki et al. (U.S. 6,611,879). The Applicant believes there is a clear deficiency in the *prima facie* case in support of the rejections, namely, the Applicant asserts that the Office Action has not shown that Muller et al. or Dobecki et al. disclose the identical invention as claimed.

It is respectfully noted that anticipation “requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*” *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). “The *identical invention* must be shown in as

complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

Claims 1-18

Regarding independent claims 1 and 10 (and claims 2-9 and 11-18 depending from them), it is respectfully noted that claims 1 and 10 relate to methods of tracking packet sequence numbers of request packets and response packets of transactions transferring data to and from a network interface, wherein both claims 1 and 10 include,

for every request packet transmitted by the network interface, writing the packet sequence number to a location in a circular send queue pointed to by a write pointer and setting a valid bit at said location, wherein the valid bit is indicative of whether at least one response is expected.

In contrast, the Muller et al. reference concerns processing of packets after they are received by a Network Interface Circuit (NIC) in order to more efficiently transfer the received packet to a host computer or other communication device. (See Muller et al. at column 8, lines 55-58). This processing aspect of received packets is further emphasized in Muller et al. at column 10, lines 32-37 which states, "In the illustrated embodiment of the invention, a communication flow comprises one or more datagram packets from one source entity to one destination entity." [Emphasis Added]

Thus, Muller et al. concerns the one way communication flow from one source entity to one destination entity, and the handling of the packets at the destination entity based on information included in the packet header for handling the packet once it arrives at the destination entity. Because Muller et al. describes the processing of received packets, Muller et al. fails to teach "for every request packet transmitted by the network interface, writing the packet sequence number to a location in a circular send queue pointed to by a write pointer and setting a valid bit at said location, wherein the valid bit is indicative of whether at least one response is expected," as recited in claims 1 and 10.

Further, Applicant's representatives fail to find in Muller et al. a teaching of "writing the packet sequence number to a location in a circular send queue pointed to by a write pointer and setting a valid bit at said location, wherein the valid bit is indicative of whether at least one

response is expected,” as recited in claims 1 and 10. The Office Action has alleged that Muller et al. shows an operational code which functions to provide information to DMA engine to assist in the re-assembly of the data packet. The Office Action further states that important flags are set to indicate more data is likely to come or not. For example, flags are checked to indicate if more data is to follow (see fig. 6B, 618-626) and operational codes indicate flows that are expected to follow (col. 44 lines 52-53 and col. 45 lines 26-35).

However, there is no teaching in Muller et al. that these various operational codes and flags are indicative of whether at least one response is expected, and further, there is no teaching in Muller et al. that these various operation codes and flag are stored at "said location" that is, a circular send queue, all as required by the recitation of both claims 1 and 10. Further, Muller et al. does not apply the “valid bit” as set forth in claims 1 and 10. Rather, Muller et al. teaches using the valid bit for error determination or correction, or as a validity indicator (*See e.g.* Muller et al. at column 37, lines 29-39), but fails to teach the validity bit used to indicate whether at least one response is expected, as required by both claims 1 and 10. In an attempt to remedy this deficiency, the pending Office Action on page 2 states, "Thus, in establishing a communication protocol it is necessary to exchange expected data (handshaking, acknowledgement, etc) in accordance to the protocol defined in the protocol header." Applicant submits that the Office Action cites no portion of Muller et al. to support these statements, and thus, the statements are mere embellishment in an attempt to supply elements recited in claims 1 and 10 that are clearly not taught in the Muller et al. reference.

Claims 19-21

Regarding independent claim 19 (and claims 20-21 depending from claim 19), claim 19 sets forth "a send queue engine" and further, "a receive queue engine partitioned from the send queue engine." These features of claim 19 as arranged in claim 19 are not shown in Dobecki et al., which uses a single packetizer/de-packetizer 428.

Applicant refers to previously presented arguments submitted in a response mailed August 17, 2004, the response submitted as responding to the Final Office Action mailed June 17, 2004. Applicant directs attention to pages 9 and 10 of the response, where it is argued that

the Dobecki et al. reference fails to teach both a send queue engine and a receive queue engine partitioned from the send queue engine, as recited in claim 19.

Applicant maintains these arguments indicating that Dobecki et al. clearly fails to teach all of the elements recited in claim 19, including the statements,

Thus, it is clear that the packetizer portion 428P and the de-packetizer portion 428D are contained in a single packetizer/de-packetizer (a single engine) 428, and are not separate as disclosed in the present specification. In fact, [on page 2 of the Final Office Action mailed June 17, 2005] the Examiner has stated "that Dobecki shows a message engine further comprising of packetizer and depacketizer [(428p, 428d, fig. 7), wherein the receive and send functions are separated]" Thus, Dobecki et al. teaches one message engine, whereas Applicant claims a receive queue engine partitioned from a send queue engine (that is, two engines).

[Emphasis in original, except for emphasis of material in square brackets, wherein all material in square brackets is added in this response for the sake of clarity and completeness].

Conclusion

Since Muller et al. fails to teach in a single prior reference a disclosure of each and every element of the claimed invention, arranged as in claims 1-18, and Dobecki et al. fails to teach in a single prior reference a disclosure of each and every element of the claimed invention as arranged in claims 19-21, claims 1-21 distinguish over the Muller et al. and the Dobecki et al. references. Thus, the 35 U.S.C. § 102 rejections of claims 1-21 cannot stand. Therefore, Applicant respectfully requests withdrawal of the rejections of claims 1-21, and an indication of allowance of claims 1-21.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JOSHUA OEN

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date Nov. 14, 2005

By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14th day of November 2005.

Amy Moriarty
Name

[Signature]
Signature